

CLAIMS

What is claimed is.

1 1. A polymer memory device comprising:
2 a series of first electrodes;
3 an array of discrete, spaced-apart polymer structures disposed over the series of
4 first electrodes; and
5 a series of second electrodes disposed over the discrete, spaced-apart polymer
6 structures.

1 2. The polymer memory device according to claim 1, wherein the first electrodes
2 have a first width, wherein the second electrodes have a second width, and wherein a given
3 polymer structure in the array of discrete, spaced-apart polymer structures has an area that is
4 greater than the product of the first width and the second width.

1 3. The polymer memory device according to claim 1, wherein the first and second
2 electrodes have a width that is a minimum feature of a photolithography technology selected
3 from 0.25 micron, 0.18 micron, 0.13 micron, and 0.11 micron.

1 4. The polymer memory device according to claim 1, further comprising:
2 a protective film disposed above and on the electrodes.

1 5. The polymer memory device according to claim 1, further comprising:
2 an organic protective film disposed above and on the electrodes.

1 6. The polymer memory device according to claim 1, wherein each electrode in the
2 series of electrodes has four rectilinear surfaces in cross-section, and wherein each electrode in
3 the series of first electrodes is contacted by the ferroelectric polymer structure on three of the
4 four surfaces.

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1 7. The polymer memory device according to claim 1, wherein the series of first
2 electrodes comprises a damascene structure disposed in a substrate.

1 8. The polymer memory device according to claim 1, wherein the array of discrete,
2 spaced-apart polymer structures further comprise a polymer selected from $(\text{CH}_2\text{-CF}_2)_n$, $(\text{CHF-}$
3 $\text{CF}_2)_n$, $(\text{CF}_2\text{-CF}_2)_n$, α -, β -, γ -, and δ -phases thereof, $(\text{CH}_2\text{-CF}_2)_n\text{-(CHF-CF}_2)_m$ copolymer, α -, β -,
4 γ -, and δ -phases thereof, and combinations thereof.

1 9. A process of forming a polymer memory structure comprising:
2 first patterning a ferroelectric polymer structure to match a first electrode layout;
3 and
4 second patterning the ferroelectric polymer structure to match a second electrode
5 layout.

1 10. The process according to claim 9, wherein first patterning further comprises:
2 patterning the ferroelectric polymer structure over the first electrode layout under
3 conditions that substantially cover the first electrode layout and that forms segmented,
4 elongated ferroelectric polymer structures.

1 11. The process according to claim 9, wherein second patterning further comprises:
2 patterning the segmented, elongated ferroelectric polymer structures by using the
3 second electrode layout as an etch mask.

1 12. The process according to claim 9, before first patterning a ferroelectric polymer
2 structure according to a first electrode layout, the process further comprising:
3 providing a substrate; and
4 forming the first electrode layout as a damascene structure in a substrate.

1 13. The process according to claim 12, after second patterning a ferroelectric polymer
2 structure according to a second electrode layout, the process further comprising:
3 forming an organic protective film above and on electrode layouts.

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1 14. The process according to claim 9, before first patterning a ferroelectric polymer
2 structure according to a first electrode layout, the process further comprising:
3 providing a substrate;
4 forming the first electrode layout upon an upper surface of the substrate.

1 15. The process according to claim 14, after second patterning a ferroelectric polymer
2 structure according to a second electrode layout, the process further comprising:
3 forming an organic protective film above and on electrode layouts.

1 16. A process of forming a memory device comprising:
2 providing a ferroelectric polymer structure between an array of intersecting lower
3 and upper electrodes; and
4 removing ferroelectric polymer material that is laterally exposed between the
5 array of electrodes.

1 17. The process according to claim 16, wherein providing a ferroelectric polymer
2 structure between an array of intersecting lower and upper electrodes further comprises:
3 providing a substrate;
4 forming the lower electrode layout;
5 forming the ferroelectric polymer structure over the lower electrode layout;
6 first patterning the ferroelectric polymer structure to form segmented, elongated
7 ferroelectric polymer structures; and
8 forming the upper electrode layout.

1 18. The process according to claim 17, wherein removing ferroelectric polymer
2 material that is laterally exposed between the array of electrodes further comprises:
3 first patterning the ferroelectric polymer structure to form segmented, elongated
4 ferroelectric polymer structures; and
5 second patterning the ferroelectric polymer structure to form discrete, spaced-
6 apart ferroelectric polymer structures.

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1 19. The process according to claim 18, wherein second patterning further comprises:
2 patterning the segmented, elongated ferroelectric polymer structures by using the
3 upper electrode layout as an etch mask.

1 20. The process according to claim 17, before first patterning, the process further
2 comprising:
3 providing a substrate; and
4 forming the lower electrode layout as a damascene structure in the substrate.

1 21. The process according to claim 18, after second patterning, the process further
2 comprising:
3 forming an organic protective film above and on electrode layouts.

1 22. The process according to claim 17, before first patterning, the process further
2 comprising:
3 providing a substrate; and
4 forming the lower electrode layout upon an upper surface of the substrate.

1 23. The process according to claim 22, after second patterning, the process further
2 comprising:
3 forming an organic protective film above and on electrode layouts.

1 24. A memory system comprising:
2 a substrate disposed on a physical interface for a host;
3 a memory article disposed on the substrate, the memory article comprising:
4 a series of first electrodes;
5 an array of discrete, spaced-apart polymer structures disposed over the
6 series of first electrodes; and
7 a series of second electrodes disposed over the discrete, spaced-apart
8 polymer structures; and
9 a signal interface for communication from the memory article to the host; and

1 25. The memory system according to claim 24, wherein the physical interface is
2 configured to a host interface that is selected from a PCMCIA card interface, a compact flash
3 card interface, a memory stick-type card interface, a desktop personal computer expansion slot
4 interface, and a removable medium interface.

1 26. The memory system according to claim 24, wherein the first and second
2 electrodes have a width that is a minimum feature of a photolithography technology selected
3 from 0.25 micron, 0.18 micron, 0.13 micron, and 0.11 micron.

1 27. The memory system according to claim 24, further comprising:
2 a protective film disposed above and on the electrodes.

1 28. The memory system according to claim 24, wherein the series of first electrodes is
2 contacted by the ferroelectric polymer structure on three of four surfaces.

1 29. The memory system according to claim 24, wherein the series of first electrodes
2 comprises a damascene structure disposed in a substrate.